CELTRO

Celtro GmbH

Job Title:	Design Engineer	**Job Category:**	IC-Design Engineering
Department/Group:	Semiconductor Development	**Job Code/ Req#:**	
Location:	Dresden	**Travel Required:**	Occasional travel
Level/Salary Range:		**Position Type:**	**Full-time employed**
HR Contact:		**Date posted:**	1.6.2023
Will Train Applicant(s):	Yes, on design-tools and development procedures	**Posting Expires:**	1.10.2023
External posting URL:	www.celtro.de		
Internal posting URL:	N.A.		

Applications Accepted By:

Fax or E-mail: +49 351 451 9842 info@celtro.de **Subject Line:** Job Description Design Engineer **Attention:** Recruiting	**Mail:** Dr. Gerd Teepe Celtro GmbH Bischofsweg 106 01099 Dresden, Germany

Job Description

Roles and Responsibilities, Activities

- Integrated Circuit Design with focus on Analog Design for novel Medical Electronics Applications
- Design/Development of new analog circuit technology (Nanowatt Power Footprint), super low leakage, low dynamic power
- Work in a startup environment in a small, responsive team, insignificant organizational hierarchy, and significant autonomy with regards to own ideas and its implementation
- Development of specification, implementation and verification of the developed solutions in the semiconductor design environment
- Mastering of Design Tools (e.g. Cadence Virtuoso or equivalent)
- Knowledge in Technology (e.g. GLOBALFOUNDRIES 22FDX or other leading edge technologies)
- Drive foundry selections and interface with semiconductor foundries. Technical emphasis is on PDK and its low power options&targets
- Cooperate seamlessly with the System Engineering

Qualifications and Education Requirements

- Diploma or Master in Electrical Engineering, Informatics or Physics
- English language (for coordination and daily work) (German language is helpful but not required)
- Basics in Program Management

Preferred Skills

- Experience in Analog / Mixed Signal Design Projects
- Development Project Experience (Basic knowledge in Project Management)
- Mastering of Analog Design Tools (e.g. Cadence Virtuoso or equivalent, training will be provided)
- Knowledge of CAD-design flows
- Knowledge in semiconductor technologies (FDSOI or FinFet) and its PDK representations
- Usage / Integration of Design IP and management of IP-Suppliers

Reviewed By:	Gerd Teepe	Date:	9. July 2023